AMENDMENTS TO THE CLAIMS

LISTING OF CLAIMS

Claims 1-36 (canceled).

37. (currently amended) A method for fabricating a semiconductor component comprising:

providing a metal leadframe comprising a plurality of leadfingers having first bonding sites on ~~having~~ a first side and second bonding sites on a second side, and a bus bar connecting at least some of the second bonding sites;

attaching a semiconductor die to the first side at least partially covering the bus bar;

~~in a chip on board configuration;~~

bonding a plurality of interconnects to the die and to the first bonding sites with the die preventing the interconnects from shorting to the bus bar; and

~~leadframe; and~~

forming a plurality of terminal contacts on the second bonding sites.

~~the leadframe on the second side.~~

38. (previously presented) The method of claim 37 further comprising forming an encapsulant on the die, on the interconnects and on the leadframe.

39. (previously presented) The method of claim 37 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

40. (currently amended) A method for fabricating a semiconductor component comprising:

providing a ~~chip on board~~ leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on a first side thereof, ~~and~~ a plurality of

terminal bonding sites on a second side thereof in an area array, and a bus bar in the area array connecting selected terminal bonding sites;

attaching a back of a semiconductor die to the leadfingers on the first side substantially covering the bus bar;

bonding a plurality of interconnects to the die and to the interconnect bonding sites with the die preventing shorting to the bus bar;

forming a plurality of terminal contacts on the terminal bonding sites; and

forming an encapsulant on the die, on the interconnects and on the leadframe.

41. (previously presented) The method of claim 40 wherein the attaching step comprises forming an adhesive member between the die and the leadframe.

42. (previously presented) The method of claim 40 wherein the forming the terminal contacts step comprises forming or attaching bumps or balls to the terminal bonding sites.

43. (previously presented) The method of claim 40 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

44. (previously presented) The method of claim 40 wherein the leadframe is contained on a strip containing a plurality of leadframes.

45. (currently amended) A method for fabricating a semiconductor component comprising:

providing a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers, a plurality of terminal bonding sites on

the leadfingers, ~~and~~ at least one bus bar electrically connecting selected leadfingers and a die mounting site formed by the leadfingers and the terminal bonding sites;

providing a semiconductor die comprising a circuit side, a plurality of die contacts on the circuit side, and a back side;

attaching the back side of the die to the ~~leadframe~~ die mounting site with the die at least partially covering the bus bar;

bonding a plurality of interconnects to the die contacts and to the interconnect bonding sites with the die preventing shorting between the bus bar and the interconnects;

~~without crossing the bus bar with the interconnects;~~

forming a plurality of terminal contacts on the terminal bonding sites; and

forming an encapsulant on the die and the leadframe.

46. (previously presented) The method of claim 45 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe.

47. (previously presented) The method of claim 45 wherein the interconnects comprise wires.

48. (previously presented) The method of claim 45 wherein the terminal contacts comprise metal bumps or balls and the terminal bonding sites are arranged in a grid array.

49. (previously presented) The method of claim 45 wherein the leadframe comprises a chip on board leadframe.

50. (previously presented) The method of claim 45 wherein the forming the encapsulant step comprises transfer molding a polymer on the die and the leadframe.

51. (currently amended) A method for fabricating a semiconductor component comprising:

providing a leadframe having a first side, an opposing second side, ~~an inner portion and an outer periphery, the leadframe comprising~~ a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers on the first side, ~~located proximate to the outer periphery,~~ a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array, and at least one bus bar in the area array electrically connecting selected leadfingers;

~~located proximate to the inner portion;~~

attaching a semiconductor die to the leadfingers on the first side at least partially covering the bus bar;

bonding a plurality of interconnects to the die and to the interconnect bonding sites with the die preventing shorting between the bus bar and the interconnects; and

forming a plurality of terminal contacts on the terminal bonding sites.

52. (previously presented) The method of claim 51 further comprising forming an encapsulant on the leadframe and the die.

53. (previously presented) The method of claim 51 wherein the interconnects comprise wires and the bonding step comprises wire bonding.

54. (previously presented) The method of claim 51 wherein the attaching step comprises forming an adhesive member between the die and the leadframe.

55. (previously presented) The method of claim 51 wherein the forming the terminal contacts step comprises forming or attaching bumps or balls to the terminal bonding sites.

56. (previously presented) The method of claim 51 wherein the leadframe is contained on a strip containing a plurality of leadframes.

57. (currently amended) A method for fabricating a semiconductor component comprising:

providing a leadframe having a first side and an opposing second side, the leadframe comprising a plurality of leadfingers having a die mounting site on the first side, a plurality of interconnect bonding sites on the first side, a plurality of terminal bonding sites on the second side in an area array and a plurality of bus bars electrically connecting selected leadfingers;

back bonding a semiconductor die to the die mounting site, the die at least partially covering the bus bars;

bonding a plurality of interconnects to the die and to the interconnect bonding sites with the die preventing shorting between the interconnects and the bus bars;

~~without crossing the bus bars with the interconnects;~~

forming a plurality of terminal contacts on the terminal bonding sites; and

encapsulating the die, the leadframe, and the interconnects in an encapsulant.

58. (previously presented) The method of claim 57 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bars are located proximate to an inner portion of the leadframe.

59. (previously presented) The method of claim 57 wherein the interconnects comprise wires.

60. (previously presented) The method of claim 57 wherein the leadframe has a chip on board configuration.

61. (previously presented) The method of claim 57 wherein the encapsulant has a chip scale outline.

62. (previously presented) The method of claim 57 wherein the leadframe has a chip scale outline.

63. (previously presented) The method of claim 57 wherein the forming the terminal contacts step comprises depositing or bonding bumps or balls to the terminal bonding sites.